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| Brigham Young University - Idaho |
| ECEN 299 – Lab 5 |
| Treble and Bass – Part 1 Schematic and Simulation, Part 2 Layout |
|  |
|  |
| **7/12/2024** |

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# Lab 5 (Part 1)

Objectives

Design a PCB for the treble & bass equalization circuits for your stereo amplifier system. Prepare Gerber files to be sent to a PCB manufacturer for fabrication. Later in the semester, when the prototypes arrive, you will be prepared to pick components for your circuit and easily measure the circuit’s performance.

# Principles to Be Studied

* Altium simulation and layout software
* Techniques to simplify debugging.

# Background

Most stereo systems have some sort of equalization, with a tone control adjustment for bass, treble, and perhaps a few mid-band adjustments as well. The design for this lab will allow you to boost (amplify) or cut (attenuate) the bass and treble frequencies by selecting specific capacitor values that allows you to control at what frequency to start boosting or cutting. Although there are many companies to choose from, we will likely use JLCPCB. JLCPCB is a manufacturer in China. You can get good quality boards for a very low price.

# Available Components

|  |  |  |  |
| --- | --- | --- | --- |
| **Item** | **Mft Part No.** | **Manufacturer** | **Description** |
| 1 | LF347DT | STMicroelectronics | IC QUAD OPAMP JFET 4MHZ 14SOIC |
| 2 | 929834-01-36-RK | 3M | CONN HEADER 36POS SNGL .100 STR |
| 3 | Miscellaneous capacitors/resistors, sizes 0603 – 1206 | | |

Table 1: Available Components

# Procedures

Figure 1 shows the overall configuration of the stereo system you are currently developing. It includes the left and right channels with the bass and treble filter circuits you are designing in this lab.

Diagram

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Figure 1 – Stereo System (Right and Left Channel) Block Diagram Redo Checkmarks.

1. Create a new project in your shared workspace titled Lab5\_TB\_Lxx\_yyy where xx is your lab bench number and yyy are your initials. If you need to review how to do this see lab 4 instructions.
2. Ensure that your projects share dialog box looks like this. See lab 4 instructions or the apendix if you get stuck.

A screenshot of a computer

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1. Now just like you did for lab 4, go ahead and create a schematic sheet and PCB Layout Document. Keep the correct name scheme for both documents (Lab5\_Sheet1.SchDoc and Lab5\_PCB1.PcbDoc)
2. Ensure everything is saved locally and to the Server (look for the green check mark specified in lab 4)

# Create a Symbol for the 23 Pin Header

These instructions are pretty much identical to the lab 4 instructions but the names, number of pins, and footprint will be different.

1. Select Panels > Project (if not already open).
2. Right click Project Group 1.DsnWrk.
3. Select Add Existing Project.
4. Browse to C:\Users\<…>\Desktop\ECEN299\ECEN299\_Library
5. Select ECEN299\_Library.LibPkg.
6. Select Open.
7. Double click on ECEN\_Library.SchLib.
8. Select Panels > SCH Library.
9. Select Add.

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1. Type ‘**23 Pin Header**’ for the Design Item ID.
2. Click OK.
3. In the SCH Library Panel, select 23 Pin Header.
4. Select Tools > Symbol Wizard.
5. Enter **23** for the Number of Pins.
6. Select ‘**Single in-line**’ as the Layout Style.
7. Enter the **pin names** in the Display Name column and select the **Electrical type** as per the figure below.

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1. Select Place > Place Symbol.
2. In the Properties window, under Parameters, ensure that 'Footprints' is selected (highlighted in blue), then click on Add... > Footprint.

1. Click on Browse and select **KBS\_23pin\_Header\_TB\_EQ**. A screenshot of a computer

   Description automatically generated
2. Select OK.
3. Select Pin Map and verify accuracy. (Make sure to verify all 23 pins match!)

A screenshot of a computer program

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1. Select OK to close Model Map
2. Select OK to close PCB Model.
3. In the Properties window, under Parameters, click on **Add... > Simulation**.
4. Select 'Browse' and locate your **DONOTHINGSPICEMODEL.CIR** file, which was created in Lab 2 (refer to Lab 2 if needed). Then select Open and OK.
5. In the Projects Window, right click **ECEN299\_Library.SchLib** and select Save.
6. Right click **ECEN299\_Library.LibPkg** and select Compile Integrated Library…
7. Save your Project.
8. In panels navigate to SCH Library. You should now see the 23 Pin Header included among the other Design Item ID’s shown here.

A screenshot of a computer program

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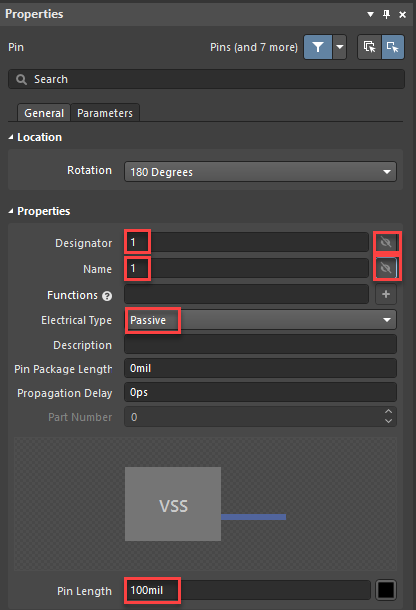
# Create a Symbol for the Capacitors

1. Select **Panels > SCH Library**.
2. Select Add.
3. Type **CMP-Capacitor** for the Design Item ID
4. Click OK.
5. Double-click on CMP-Capacitor to open its properties if they are not already open.
6. In the Properties panel, set the following settings as shown below.

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1. Press the g key to cycle through grid spacing. Stop on **Grid: 10mil**. To see the current grid spacing look at the bottom left of the program.
2. Select Place > Pin.
3. Press the ‘Tab’ key to change the properties of the pin.
4. Set the following properties as shown below for the first pin.



1. When placing the pin, ensure the designator points outward from your symbol, as it will be used to connect your capacitor to other components/sources.

A red arrow pointing at a line

Description automatically generated

1. Place the **first** pin at **X:** -**100mil** and **Y:** **0mil**.
2. Place the **second** pin at **X: 200mil** and **Y:** **0mil** (Note: you will need to flip the pins orientation to point the designator outwards**).**

A black and white grid

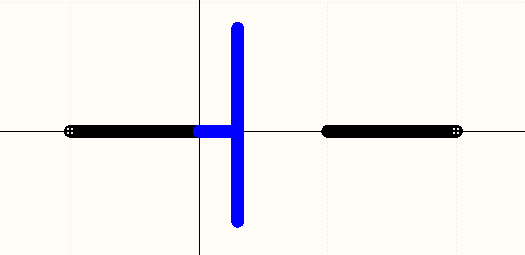
Description automatically generated

1. Right click to exit placing a pin. Select **Place > Line**.
2. Press the ‘Tab’ key to change the properties of the Line.
3. Change the line color to blue.

A screenshot of a computer

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1. Click the Pause button in the middle of the screen.
2. Start drawing a horizontal line from **X: 0 mil**, **Y: 0 mil** to **X: 30 mil**, **Y: 0 mil.**
3. Then, draw a vertical line from **Y: 80 mil** to **Y: -70 mil** at **X: 30 mil**.

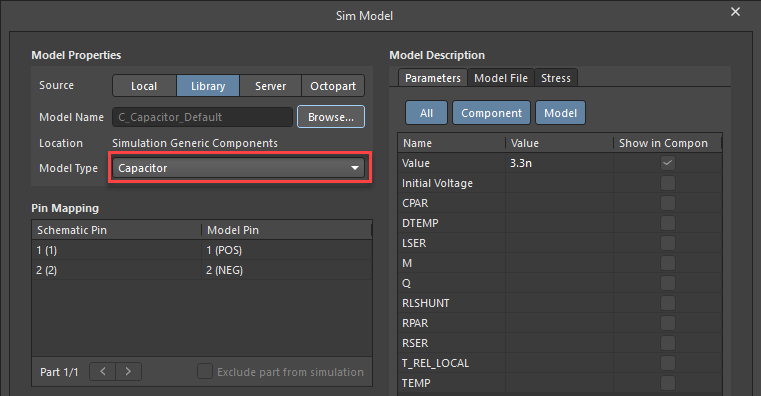


1. Draw another horizontal line from **X: 100 mil**, **Y: 0 mil** to **X: 70 mil**, **Y: 0 mil**.
2. Then, draw another vertical line from **Y: 80 mil** to **Y: -70 mil** at **X: 70 mil**.

A blue lines on a white background

Description automatically generated

1. Then, select SCH Library > CMP-Capacitor
2. If the Properties panel is not opened for the CMP-Capacitor, select Panels > Properties.
3. Next, choose Add... > Parameter.
4. Double-click 'Parameter' and rename it to 'Value.'
5. Double-click '\*' and set the capacitor's default value to 3.3n.
6. Make the value visible by clicking on the eye icon.
7. Click on Add… > Footprint.
8. Click on Browse and select **KBS\_SMD0603**
9. Select OK.
10. Repeat steps 27 to 29 to add the **KBS\_SMD0805** and **KBS\_SMD1206** footprints.
11. Select Add… > Simulation.
12. Select 'Capacitor' for the Model Type.



1. Select OK.
2. In the Projects Window, right click **ECEN299\_Library.SchLib** and select Save.
3. Right click **ECEN299\_Library.LibPkg** and select **Compile Integrated Library**…

## Designing the Treble and Bass

**Figures 2** and **3** illustrate one channel of the bass and treble filter circuits you will design and implement in your stereo amplifier system. You will need to duplicate the circuits in both figures for the left and right channels. Ensure that every resistor, potentiometer, and capacitor has a unique designator.

Note that bLpot and tLpot, Fig. 2 and Fig. 3, are located on the chassis but you need them for simulation purposes.

1. To get the potentiometer, **select Components > Simulation Generic Components**. Then look for potentiometer in the search field.

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1. In the Properties panel of the potentiometer, rename the **Designator** field as needed (e.g., bLpot for the bass left channel) and set the **value** to **10k**, matching the potentiometers already mounted in your chassis.

A diagram of a circuit

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Figure 2 – Bass Tone Control (one channel)

A diagram of a circuit

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Figure 3 – Treble Tone Control (one channel)

Table 2 provides the signal names and pin numbers for the 23-pin header. Be careful to label your nets correctly. Miss labeled nets is one of the most common problems in layouts.

Table 2 Signal Names and Pin numbers for the 23-pin header.

|  |  |  |
| --- | --- | --- |
| **Signal Name** | **Pin #** | **Description** |
| bLin | 1 | Left channel Bass input |
| bRin | 23 | Right channel Bass input |
| P1S | 3 | Source impedance side pot terminal for bass (L) |
| P2S | 21 | Source impedance side pot terminal for bass (R) |
| P1W | 5 | Wiper terminal for bass pot (L) |
| P2W | 19 | Wiper terminal for bass pot (R) |
| P1F | 7 | Feedback impedance side pot terminal for bass (L) |
| P2F | 17 | Feedback impedance side pot terminal for bass (R) |
| P3S | 6 | Source impedance side pot terminal for treble (L) |
| P4S | 18 | Source impedance side pot terminal for treble (R) |
| P3W | 4 | Wiper terminal for treble pot (L) |
| P4W | 20 | Wiper terminal for treble pot (R) |
| P3F | 2 | Feedback impedance side pot terminal for treble (L) |
| P4F | 22 | Feedback impedance side pot terminal for treble (R) |
| bLout | 11 | Left channel Bass output |
| bRout | 13 | Right channel Bass output |
| tLin | 8 | Left channel Treble input |
| tRin | 16 | Right channel Treble input |
| tRout | 14 | Right channel Treble output |
| tLout | 10 | Left channel Treble output |
| V+ | 9 | Positive power rail |
| V- | 15 | Negative power rail |
| GND | 12 | Ground |

## PCB Tester Compatibility

Verify that your design is compatible with the PCB Tester that was created at BYU-Idaho that can check for shorts and opens in your PCB after it is fabricated. To be compatible with the tester, assign the op amps in your circuit using the instructions in Fig 4.

A picture containing chart

Description automatically generated

Figure 4 – Op Amp Selection Guild for compatibility with PCB Tester

# Calculate Expected Bass and Treble Gains

The circuit design allows you to either boost or cut low or high frequencies within the audible range. Let’s calculate the expected gain for both the bass and treble circuit at low and high frequencies and for the control knobs turned all the way down and all the way up.

When analyzing the potentiometer in the context of the circuit, you need to split it into separate resistors, as shown in Fig. 5. The value of corresponds to the wiper position within the potentiometer. When, the knob is turned fully clockwise. When, the knob is turned fully counterclockwise. When, the knob is at the center position.

Diagram

Description automatically generated with low confidence

Figure 5 – Equivalent Potentiometer Circuit

# Bass

The gain equation (also called the transfer function) for the bass circuit and components values needed to meet the design specifications are shown in Appendix A. Using Appendix A Summary and Worksheet, evaluate the gain of the circuit at and with the potentiometer set position at (cut) and (boost) and record these values in Table 3. Note that at these two frequencies, the capacitor impedance can be replaced with either an open () or short () circuit.

Table 3 Bass Filter Circuit Frequency Response Calculations.

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How does this analysis support the claim that the circuit will act as a bass tone control?

Use the component values derived in Appendix A. The potentiometer is already mounted in your chassis. Simulate this circuit in Altium Designer to verify that you get the desired frequency response.

## Simulate the Circuit

1. Create two DC sources into your schematic: one set at **+14 volts** and the other at **-14 volts** to supply power to the Op-Amp.

A diagram of electrical wiring

Description automatically generated

1. Add a Sinusoidal source to bLin with an AC Magnitude of **1 V.**

A screenshot of a computer

Description automatically generated

1. Select Simulate > Simulation Dashboard.
2. To set up parametric sweep for the bLpot potentiometer, select Sweep and then click on Settings.

A screenshot of a computer program

Description automatically generated

1. Enter the following Sweep parameters values:

A screenshot of a computer

Description automatically generated

1. Select OK.
2. Create a Frequency Analysis by expanding the AC Sweep section.
3. Set Start Frequency to 20 and End Frequency to 20k.

A screenshot of a computer program

Description automatically generated

1. Add **bLout** as your Output Expression. Ensure the complex functions are set to **Magnitude (dB)** as shown below when adding the output expression.

A screenshot of a computer

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1. Select Create.
2. Select Simulate > Run Simulation
3. In the Top Menu, select Simulate > Generate Netlist.
4. Find the Sweep line:

A screenshot of a computer program

Description automatically generated

1. Modify the line to add [position] after bLpot.

A screenshot of a computer program

Description automatically generated

1. Select **Simulate > Run**. If it does not open, check Panels > Messages for any error messages.

**Figure 6** and **Figure 7** plot the typical frequency responses you can achieve with this circuitry. Each curve in the plot represents a different setting of the bass or treble control. Notice that they can be set for a flat (no boost or cut) response.

A screenshot of a computer

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Figure 6 – Bass Control Frequency Response

# Treble

We will now develop a more detailed analysis of the circuit performance that will help us complete the design. For a maximum boost setting, when and when.

The gain equation (also called the transfer function) for the treble circuit is shown in Appendix B and is derived by using KCL to sum the currents into each of the potentiometer nodes.

Using Appendix B Summary and Worksheet, evaluate the gain of the treble circuit at and with the potentiometer set position at (cut) and (boost) and record your results in Table 4. At these two frequencies, the capacitor impedance can be replaced with either an open () or short () circuit.

Table 4 Treble Filter Circuit Frequency Response Calculations.

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How does this analysis support the claim that the circuit will act as a treble tone control?

## Simulate the Circuit

You will now simulate this circuit in Altium Designer to verify that you get the desired frequency response.

1. Add a Sinusoidal source to tLin with an AC Magnitude of **1 V**
2. Delete the previous Output Expression **(dB(v(bLout)).**
3. Add **tLout** as your Output Expression. Ensure the complex functions are set to **Magnitude (dB).**
4. Change the Sweep Parameter from bLpot to tLpot as shown below.

A screenshot of a computer

Description automatically generated

1. Follow steps 11-15 from the previous Bass Section to complete the simulation.

A screen shot of a graph

Description automatically generated

Figure 7 – Treble Control Frequency Response

Take screenshots of both simulations and add them to your lab report**.**

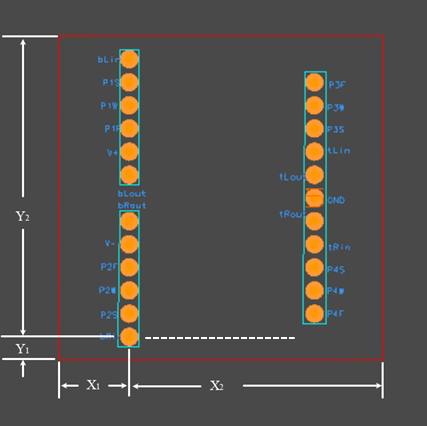
Have a lab assistant or the professor check your schematic before moving on to Layout. Include in your lab report who checked your schematic.

# Lab 5 (Part 2)

# PCB Layout

**For any questions on how to create a layout, see the previous labs.**

The figure below shows the **maximum dimensions** for the board outline for the Mixer PCB to fit into the chassis. The figure is not to scale. **Smaller is typically better** for ease of inserting the header pins, but the maximum values should not be exceeded.:



in. **max**., in. **max**., in. **max**., in. **max.**

* 5 Extra Credit Points for traces on one side and ground plane on other. (Including research on what a ground plane is. The extra credit will be given when your write-up is included in Lab 9).

As in previous labs, zip your Gerber and NC drill files. If you want to check these files with Gerbv, see document called “How to Grade Layouts” (It is getting updated right now from pads to Altium) attached to Lab 4 and Lab 5 (This is how the TA’s grade your PCB’s).

Go to <https://jlcpcb.com/> and upload your Gerber files. Make sure they look correct. Take screenshots of this and add them to your lab report**.**

The grading rubric can be found on I-Learn. If your board contains errors that we catch, you will be asked to correct those errors and resubmit before your board will be fabricated.

Submit your Gerber and NC drill files as a single zip file with your given names as the file name. **You will not submit a lab report now since it will be incorporated later when you submit your Lab 9 written lab report.**

# Things to remember for Lab 5:

* Take notes of the things you did wrong in Lab 4 and try to avoid making those same mistakes!
* Use the correct Library. That will help you to make sure you are using the correct parts with the correct Footprints and Symbols.
* Set your trace, via and clearance constraints correctly, and do it before routing. That will help you to keep a clearance of 10 mils between your pads and traces.
* Don't place your text or reference designators on resistor pads, header pin pads, op-amp IC pads, or vias. There is no problem with placing your text or references designators over your traces.
* Make sure your text and reference designator sizes are correct. The height of the text should be 40 mil and the width, 6 mil. If you make it too small or narrow, JLCPCB says that your characters will be unidentifiable.
* When you generate your Gerber files, make sure they have the content they are supposed to have. If you have questions about how to check your Gerber files, you can ask a Lab Assistant. You can also download Gerbv at <http://gerbv.geda-project.org/>. This program allows you to view all your Gerber files separately.
* Make sure that your zip file contains both Gerber and NC Drill files.
* Make sure that the footprints of your resistors, Op Amp and capacitors look alright. (i.e use that right footprint size according to your lab kit)
* Make sure that your board size and the distance between your header pins and your board outline are correct. You can use the Distance tool to measure your distances by using Ctrl M
* Remember to add a ground plane.
* Remember to include the names of both lab partners on your board (On the Top Overlay layer).
* Check that all your header pins are connected to their respective resistors by looking at your schematic along with your layout at the same time. If some of your header pins aren't connected to any resistors or anything, that means some of your connections in your schematic weren't made correctly. Check for components that are not connected properly or for paths that have the same name or reference designator. You shouldn't have repeated path names.

Once your Lab 5 layout is complete, you can use this checklist of things to remember above and the rubric to verify that you have met these requirements.

## Grading Rubric

|  |  |
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| **Grading Rubric** | |
| **Worth** | **Description** |
| 15 | Overall Board Quality  Layout looks organized and clean, conservatively saves board space, utilizes both sides of the board, cells and ref. des. were placed purposefully. |
| 15 | Reference designators are present, descriptive, and placed appropriately |
| 15 | Correct Trace Widths (10 mils) |
| 15 | Size Constraint  Is within the allowed maximum dimensions. |
| 10 | 10-pin header is placed within allowed limits of the board outline |
| 10 | All Gerber files are present and have correct content.  The NC Drill file (.ncd) shows drill holes lining up with holes, vias, and header pins. |
| 10 | Include the names of each group member on the board |
| 5 | Hole, Vias, and Cells correctly sized |
| 5 | NC Drill (.ncd) file in the same folder as the other Gerber files. |
| **100** | **Total** |

# Appendix A – Bass Transfer Function and Selecting Component Values

Diagram, schematic

Description automatically generated

The transfer function for the bass circuit is derived in the textbook on page 606 (11ed) as

This can be rewritten as

Thus, the Bass Transfer function can be written as

|  |
| --- |
| where |

From this transfer function, we can solve for component values that will meet the specifications.

**1. To meet the specification of**  at high frequency with , then

Since ,

Therefore, let

**2. To meet the specification of**  atwith a = 1, then

That is

Therefore, let

Nominally, this will set the corner frequency to

## Appendix A Summary and Worksheet - Bass Transfer Function:

Diagram, schematic

Description automatically generated

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# Appendix B - Treble Transfer Function and Selecting Component Values

Diagram, schematic

Description automatically generated

1. The transfer function for the Treble Amplifier Circuit, shown above, is

|  |  |
| --- | --- |
| where | Eqn. 11 |

From this transfer function, we can solve for component values that will meet the specifications.

**1. To meet the specification of**  at high frequency with **a = 1**, then

Thus,

**2. To meet the specification of**  atwith a = 1, then

That is

These two constraints can then be used to find values for that will meet desired specifications

From the first constraint,

Letting and , yields

Thus, let .

From the second constraint,

Thus, let

|  |
| --- |
| Reference only: The potentiometer is already mounted in your chassis. Resistors and allow for necessary [input bias current](http://www.analog.com/static/imported-files/tutorials/MT-038.pdf). To understand how and affect the circuit, redraw it with the capacitor either shorted or open (depending on the frequency) and the potentiometer drawn as shown in Figure 5. |

## Appendix B Summary and Worksheet - Treble Transfer Function

### Treble Circuit

Diagram, schematic

Description automatically generated

Treble Transfer Function:

where

and

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## Appendix C

## Edit *Shared with* Project Options

Share with

1. Select Panels > Explorer.
2. Select Folders tab at the bottom.
3. Expand the ECEN299\_S24 > Lxx folder where xx is your lab bench number.
4. Select your Lab4\_PAM\_Lxx\_yyy project.

A screenshot of a computer program

Description automatically generated

1. Select Share.

### Share with ECEN299\_Lxx = Can Edit

1. Expand Shared with.
2. Select Remove next to Workspace Members.
3. Enter ECEN299\_Lxx in the Enter email or name field.
4. Select ECEN299\_Lxx (role).

This is a role that is assigned to you and your lab partner.

A screenshot of a computer

Description automatically generated

1. Select the eye icon and select Can Edit.
2. Select Share.

A screenshot of a computer

Description automatically generated

### Share with Workspace Members = Remove (None)

1. Select Who has access.
2. Select Can Edit for ECEN299\_Lxx (if not already selected).
3. Select Remove for Workspace Members.

A screenshot of a computer

Description automatically generated

This will permit only you and your lap parent to edit the project.

1. Select Save.

### Share with ECEN299\_S24\_TA = Can View

1. Select Who has access.
2. Enter ECEN299\_S24\_All in the Enter email or name field.
3. Select ECEN299\_S24\_All (role).
4. Select the eye icon and select Can View. (if not already selected)
5. Select Share.

The Share dialog box should look like this:

A screenshot of a computer

Description automatically generated

1. Select OK to close Share “Lab4\_PAM\_Lxx\_yyy”.

## To Open Your Lab Partner’s Workspace Project

1. Open Altium Designer.
2. Sign in and select a license.
3. Select the BYUI Workspace server (top left).
4. Select Panels > Projects.
5. Select File > Open Project.

A screenshot of a computer

Description automatically generated

1. Select the pulldown menu next to Open.

A screenshot of a computer

Description automatically generated

1. Select Open to custom path.
2. Browse to %UserProfile%\Desktop\ECEN299.
3. Click Select Folder.

The Project is copied locally and is linked to the server.